IN THE CLAIMS

Please cancel claims 4-5, 12, 18, and 23-24 without prejudice.

Please amend claim 21 and the first instance of original claim no. 16 as follows below.

The following listing of claims replaces all prior versions, and listings, of claims in the application:

Marked-up Listing of Claims

1. (Original) A processor comprising:

a protected execution unit to process instructions;

a check unit to detect an error associated with processed instructions; and

a replay queue to issue instructions to the protected execution unit for processing, track the issued instructions, and reissue selected issued instructions when the check unit detects an error.

2. (Original) The processor of claim 1, wherein instructions are flushed from the execution unit when the check unit indicates an error.

3. (Original) The processor of claim 1, wherein the replay queue includes first and second pointers to indicate a next instruction to issue and a next instruction to retire.

4. (Cancelled)

5. (Cancelled)

6. (Original) The processor of claim 1, wherein the execution units operate in lock step when the processor is in a high reliability mode and the execution units independently when the processor is in a high performance mode.

7. (Original) The processor of claim 1, wherein the processor implements a recovery algorithm if an instruction that triggers a replay generates a mismatch when it is replayed.

8. (Original) A method for executing instructions with high reliability, comprising:

storing an instruction temporaily in a replay buffer;

issuing the instruction to a protected execution unit;

checking results generated by the instruction in the protected execution unit; and

reissuing the instruction to the protected execution unit if an error is indicated.

9. (Original) The method of claim 8, wherein issuing the instruction comprises:

staging the instruction to the protected execution unit; and

adjusting a first flag in the buffer to indicate the instruction has been issued.

10. (Original) The method of claim 8, wherein adjusting the first flag comprises setting a first pointer to indicate a buffer slot in which the issued instruction is stored.

11. (Original) The method of claim 10, further comprising setting a second pointer to indicate a buffer slot in which a next instruction to retire is stored.

12. (Cancelled)

13. (Original) The method of claim 8, further comprising retiring the instruction when no error is indicated.

14. (Original) The method of claim 13, wherein retiring the instruction comprises:

adjusting a second pointer to indicate the instruction has retired; and

updating an architectural state data with the result generated by the instruction.

15 [[16]]. (Currently Amended) A computer system comprising:

a processor that includes:

a protected execution unit to execute instructions in a manner that faciliates soft error detection;

a check unit to monitor the protected execution unit and to generate a signal when an error is indicated;

a replay unit to provide instructions to the protected execution unit, track the instructions until they are retired, and replay selected instructions when the check unit indicates an error; and

a storage structure to provide a recovery algorithm to the processor when replay of selected instructions does not eliminate the mismatch.

16. (Original) The computer system of claim 15, wherein the replay unit includes first and second pointers to indicate a next instruction to issue and a next instruction to retire, respectively.

17. (Original) The computer system of claim 16, wherein the execution units are flushed prior to the replay when an error is indicated.

18. (Cancelled)

19. (Original) The computer system of claim 16, wherein the storage structure is a non-volatile memory structure.

20. (Original) The computer system of claim 15, wherein the protected execution unit comprises first and second execution units and the replay unit provides identical instructions to the first and second execution units.

21. (Currently Amended) A processor comprising:

first and second execution cores to process identical instructions in lock step, each execution core including a replay unit to track instructions that have yet to retire; and [[.]]

a check unit to compare instructions results generated by the execution cores and to trigger the replay unit to resteer the first and second execution cores to an instruction when the instruction results generate a mismatch.

22. (Original) The processor of claim 21, wherein each replay unit includes buffer slots to store instructions for execution and first and second pointers to indicate a next instruction to issue and a next instruction to retire, respectively.

23. (Cancelled)

24. (Cancelled) .